

REMARKS

The objections to the specification and claim 5 are attended to by amendments above. The amendments to claim 5 are all non-narrowing edits that do not invoke any present Festo decision.

The references cited against Claim 1 for obviousness under 35 USC §103 (a) were Chun, et al. (U.S. Pat. No. 6,133,727), in view of Jiang, et al. (U.S. Pat. No. 4,654,829) and Phan, et al. (U.S. Pat. No. 6,367,042). However, there are a number of substantial differences between the invention of Claim 1 and the Chun, Jiang, and Phan et al. patents.

The primary object of the invention of Claim 1 is to provide a method for testing a non-volatile memory, which can verify whether the code written in the memory is the same as the one assigned by the client.

Another object of Claim 5 is to provide a method for testing with a non-volatile memory whether code retrieved by the controlling program of a testing machine is correct.

Compared with the present invention, the Chun, et al. patent focuses on comparing the test data with the reference data to determine whether the tester is functionally stable (verify the tester's accuracy). Not only the Chun, et al. patent, but also the Jiang, and Phan, et al. patents cannot achieve the objectives of the present invention.

According to the Abstract of the Phan, et al. patent, the integrated circuit die includes a fuse array or other circuitry capable of storing an identification number, an embedded memory and built-in self-test (BIST). The identification number is encoded to differentiate the die from the others, and test results (tested by the BIST) are associated with a particular die via the identification number of the die. In fact, the identifiers of the dies are only used to identify the dies themselves, but not used for testing purposes, as claimed. The present

invention, the code assigned by a client is used for testing purpose rather than as an identifier.

According to the specification of the Chun, et al. patent (Col. 1, lines 65-67; Col. 2, lines 1-47), it substantially discloses a semiconductor device tester having a check-tester mode for verifying the correct operation mode for the tester and a standard-device-creation mode. Although the purpose of the check-tester mode is similar to step (d) of Claim 1, the Chun et al. patent focus on comparing the test data with the reference data differently determines whether the tester is functionally stable. On the contrary, the objective of the present invention is to verify the tester program. The present invention checks if the code retrieved by the controlling program is incorrect and if the code written in the memory is the same as the one assigned by the client. They are different in whole.

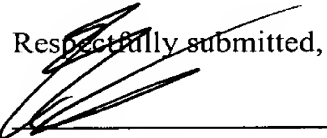
In the check-mode of the Chun, et al. patent, it is only disclosed that if the candidate device is judged as a standard device, the serial number initially accorded to it is marked on the device for future identification (Col. 5, lines 15-18). As with the Phan, et al. patent, the Chun, et al. patent also does not teach the method of testing a non-volatile memory via the code assigned by a client, i.e. they do not disclose step (c) Claim 1 or Claim 5 of the present invention.

As above stated, the Chun, et al patent does not disclose the method to verify if the code written in the memory is assigned by the client or not, even in view of the Phan and Jiang, et al. patents. In fact, the method taught by them is more similar to the code testing described in "Description of the prior art" of the present invention.

The present invention should not be confused with a normal code testing. The method of Claim 1 cannot be made by a person having ordinary skills in the art based on the cited references.

With respect to Claims 2-4 and 6, the Examiner rejected them with parent claims, Claim 1 and Claim 5. However, since Claim 1 and Claim 5 have novelty and non-obviousness as described above, then Claims 2-4 and 6 have novelty and non-obviousness, too. Reconsideration and allowance are, therefore, requested.

Respectfully submitted,



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